PRN:		Course Code :	ECE403

Final Year **B. Tech** End Semester Examination Summer 2023

VLSI System Design

Day and Date: Wednesday, 14/06/2023 **Max Marks:** **100**

Time : 2-00 to 5.00 pm **Duration:** **03** hrs

Instructions: All questions are compulsory.

			Marks	Bloom's Level	CLO
Q.1		**Attempt the following**			
	a)	With neat and suitable block diagram, explain VLSI design flow.	08	2	1
	b)	Which are the different types of 'Operators' that operate on signals variables and constants in VHDL? Summarize all types. Elaborate 'Logical' operators.	08	2	1
		OR			
	b)	Explain briefly the different levels of abstraction.	08	2	1
Q.2		**Attempt the following**			
	a)	Write VHDI- code for 4:1 multiplexer.	08	6	2
	b)	Write a VHDL code to realize 2-bit Comparator	08	6	2
		OR			
	b)	Write a VHDL code to realize SR-FlipFlop.	08	6	2
Q.3		**Attempt any two from the following**			
	a)	Draw and explain the voltage transfer characteristics of CMOS inverter.	08	2	3
	b)	Explain Noise Margin of CMOS Inverter	08	2	3
	c)	Draw and explain Enhancement mode Transistor action	08	2	3
Q.4		**Attempt any two from the following**			
	a)	State CMOS design methodology and design CMOS inverter (NOT) gate.	08	6	2
	b)	Design two input NAND gate and explain operation	08	6	2
	c)	Design Half adder circuits (CMOS Technology)	08	6	2

ESE Backlog

SGU Library Copy

Q.5	**Attempt any Two of the following**				
	a)	Write a Verilog code to realize Binary to Gray Code conversion	09	6	2
	b)	Explain Verilog data types	09	3	2
	c)	Explain structural hierarchical description of 16-to-1 multiplexer.	09	2	1
Q.6	**Attempt any Two of the following**				
	a)	Explain Spartan-III FPGA (XC3S400) architecture.	09	2	3
	b)	Write a note on Boundary Scan	09	2	3
	c)	State different FPGA Programming Technologies and explain any one.	09	2	3

*****

ESE Backlog